Microfluidic vias enable nested bioarrays and autoregulatory devices in Newtonian fluids

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We report on a fundamental technological advance for multilayer polydimethylsiloxane (PDMS) microfluidics. Vertical passages (vias), connecting channels located in different layers, are fabricated monolithically, in parallel, by simple and easy means. The resulting 3D connectivity greatly expands the potential complexity of microfluidic architecture. We apply the vias to printing nested bioarrays and building autoregulatory devices. A current source is demonstrated, while a diode and a rectifier are derived; all are building blocks for analog circuitry in Newtonian fluids. We also describe microfluidic septa and their applications. Vias lay the foundation for a new generation of microfluidic devices.

autoregulation | microelectromechanical devices | polydimethylsiloxane | array | logic

Over the decade of its existence, polydimethylsiloxane (PDMS) microfluidics has progressed from the plain microchannel (1) through pneumatic valves and pumps (2, 3) to an impressive set of specialized components organized by the thousands in multilayer large-scale-integration chips (4). These devices have become the hydraulic elastomeric embodiment of Richard Feynman's dreams of infinitesimal machines (5, 6). The now established technology (7) has found successful applications in protein crystallization (8), DNA sequencing (9), nanoliter PCR (10), cell sorting and cytometry (11), nucleic acids extraction and purification (12), immunoassays (13, 14), cell studies (15–18), and chemical synthesis (19), while also serving as the fluid-handling component in emerging integrated microelectromechanical devices (MEMS) (20).

The energetic pursuit of applications, however, has resulted in a premature attention shift away from fundamental microfluidics. Here we report on a fundamental technological advance that allows a simple and easy access to a large increase in the architectural complexity of microfluidic devices, as well as opens new possibilities for technical developments and consequent applications. We dubbed the previously undescribed device "via," in reference to its analog in modern semiconductor electronics.

Vias are vertical micropassages that connect channels fabricated in different layers of the same PDMS multilayer chip. The functional result is 3D channels that lift the restrictions of the traditional architecture wherein channels could not leave their layer and two channels within the same layer could not cross without mixing. These restrictions did not prevent the emergence of expansive architectures (4), because the particular applications were shrewdly chosen to involve large-scale parallelization of simple identical operations, thereby requiring few controls and maximizing device density. However, as the field moves to functionally complex heterogeneous devices integrated on the same chip, laying out the respective circuitry would inevitably necessitate convenient, simple, and reliable vertical connectivity just as it did in the semiconductor industry. Microfluidic vias provide that 3D connectivity, lift the above architectural restrictions, and contribute morphological and functional capabilities.

The pursuit of 3D devices is not new. Whitesides and colleagues at Harvard University (21) developed an ingenious scheme wherein a complex system of multilayer photoresist molds, photoresist premasters, and PDMS masters were fabricated and then used in an involved many-step process to produce a 70-μm-thick PDMS layer housing 100-μm-wide vertical cylinders connecting 70-μm-tall channels fabricated in thick PDMS slabs. The resulting 3D technique was successfully used in protein and cell patterning (22). Jo *et al.* (23) demonstrate a similar method involving physical clamping to control layer thickness. Whitesides and colleagues (24) also developed a technique to produce 3D channels by mechanical deformation of straight channels. However, the challenging and labor-intensive fabrication of the above devices has largely dissuaded researchers from further work with these methods.

On the other hand, the fabrication of vias presented here is as simple, fast, and easy as the one of standard multilayer devices, thereby removing the practical obstacles to the wide use of 3D microfluidic architectures. In addition, vias can work with significantly smaller dimensions, e.g., 7-μm-tall channels connected by 25-μm-wide vias. The ultimate limit in miniaturization is now set by the submicrometer resolution of optical lithography, rather than the softness of PDMS masters.

Via Fabrication and Architecture

The flow chart of via fabrication is shown in Fig. 1. PDMS is spun onto a standard hybrid mold to a thickness smaller than the height of the taller features, but larger than the height of the shorter features. As a result, the taller features protrude through the upper PDMS surface. After curing, a separately fabricated layer is assembled on top in such a way that the end of its channel matches the protruding mold feature. After bonding, the device is peeled off and assembled to a substrate, e.g., a glass slide. Stacking the two PDMS layers in this fashion produces a vertical connection (via) between channels fabricated in each layer. The functional result is a composite channel that switches from one layer to another as it winds its way through the chip. Fig. 2 contains photos of actual via devices.

If two such devices are combined, an "overpass" or "underpass" is produced (Fig. 3). They allow two channels traveling in the same layer to cross without mixing, because one of the channels switches over to an adjacent layer for the length of the crossing. Overpasses and underpasses can be arranged in series to enable 3D flexibility in the architectural layout of a two-layer chip.

Further enhancements are possible by increasing the number of stacked PDMS layers. Up to seven layers have been reported bound by optimized thermal curing procedures (2), whereas

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Abbreviations: MEMS, microelectromechanical devices; PDMS, polydimethylsiloxane.

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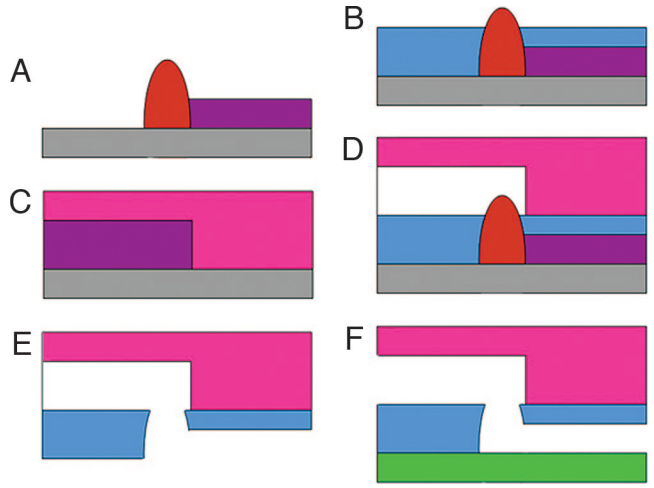

Fig. 1. Via fabrication (drawing not to scale). (*A*) Standard hybrid mold is constructed by using Su8 (violet) and Az50 (orange) photoresists spun at 7- and 30-μm heights, respectively. The mold is then baked at 200°C for 1 h to round the Az50 features. (*B*) 20:1 uncured PDMS (blue) is spun at 4,000 rpm so that the high features protrude through and over the PDMS surface. (*C*) 5:1 uncured PDMS (pink) is poured over another mold. *B* and *C* are partially cured at 80°C for 30 min. (*D*) The *C* layer is peeled off and assembled onto the *B* layer. Curing is completed to bond the layers. (*E* and *F*) The chip is peeled off the *A* mold (*E*) and assembled to a substrate of choice (green) (*F*). In the resulting device, the via connects channels fabricated in different layers.

alternative binding schemes, e.g., oxygen plasma treatment, should allow even larger stacks. The multilayer stacking would be produced by binding a Fig. 1*E* structure to a Fig. 1*B* structure, peeling off the mold, and iterating. The final lowest elastomeric layer would be bound to a substrate. Multiple layers carrying channels interconnected with vias open an enormous phase space of architectural possibilities to explore in future devices and applications.

To determine the optimal via fabrication parameters, we created a two-layer matrix containing four independent sets of 3D channels assembled by 288 vias of lateral dimensions that systematically vary between 25 and 80 μm, in 5-μm steps. A number of chips at different thicknesses of the lower PDMS layer were produced by using different spin speeds. Optimal results were achieved for 4,000 rpm (on a 3-inch wafer) and via lateral dimensions between 50 and 65 μm, where vias formed successfully and reproducibly.

For some devices of larger dimensions and/or lower spin speeds, surface tension of the uncured PDMS formed a hump over the tall mold features. That hump cured into an unbroken membrane, producing a defective via. At smaller lateral dimensions, melting the photoresist during the rounding process lowered the height of the tall mold features. Thus, they were too short to break through the subsequent PDMS layer.

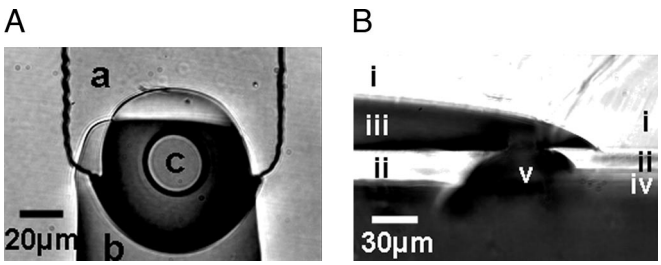

Fig. 2. Rounded via devices. (*A*) Top view shows lower (a) and upper (b) channels and via (*c*). The access annulus is clearly visible. (*B*) Side-view cross-section shows upper (i) and lower (ii) layers, upper (iii) and lower (iv) channels, and via (v). The chip was peeled off the glass slide, cut with a razor, and laid on its side to take the photograph. Compare with Fig. 1*F*.

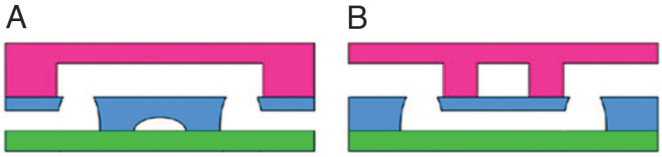

Fig. 3. Two copies of the device from Fig. 1 can be combined to produce an overpass (*A*) or an underpass (*B*). They allow two channels traveling in the same layer to cross without mixing because one of the channels jumps to an adjacent layer for the length of the crossing. A series of such structures allows full 3D flexibility of architectural layout of the chip's channels, accomplished by simple means.

Microfluidic Septum

The incomplete formation of vias at lower spin speeds and/or extreme dimensions suggested another device: a microfluidic septum. The flow chart of its fabrication mimics that of the via, except for spinning the PDMS slightly above all features of the hybrid mold. Another way to think about a septum is as a purposefully defective via.

The septum has the useful property that it would breach at a characteristic pressure determined by its fabrication parameters. For example, an 80 $\times$ 80-μm septum at 3,000 rpm on a 3-inch wafer over a 36-μm-tall rounded mold breaches at 5 psi. Therefore, a septum can be used to isolate a certain section of the chip, up to a specific applied pressure. Such "destructive engineering" has been demonstrated by using voltage instead of pressure (25).

In industrial chip packaging, a septum could keep dust out, or reagents in, until the sealed section is to be accessed. Also, if the sealed section is connected to an exhaust vent, then the septum acts as an irreversible microfluidic fuse. When the applied pressure exceeds a certain hardwired value, the septum breaches, the fluid flows to the exhaust, and the pressure decreases. This scheme can be used to protect a sensitive section of the chip against excessive pressures.

If a system of septa tuned to different breaching pressures is built within the same chip, then the chip could be configured to varying final functionalities by applying respective pressures. This technique would allow mass-production of identical chips that could later be finalized to suit specific needs. Each chip would then be operated at pressures too low to cause further architectural changes. Such chips could be arranged in a system (20) to build fluidic analog computers impervious to electromagnetic pulse.

Nonrounded Vias

All vias discussed up to this point were made by using rounded molds. Hence, we next fabricated devices by using nonrounded (or square-profile) molds of the same 288-via layout. Virtually all vias of 25- to 80-μm lateral dimensions formed successfully at 2,500 rpm on 3-inch wafers. Fig. 4 *A* and *B* shows 25-μm-square functional vias. The lack of melting preserves the height of the narrow features, whereas the sharp edges help break the PDMS surface tension, thereby explaining the greater success of this technique.

To demonstrate the correct workings of the chip, the four independent sets of channels were filled with solutions containing plain buffer, fluorescein, Cy3, or Cy5 dyes. One colorless image and the respective three fluorescence images were mixed in false color to produce Fig. 4*C*. Of the 288 sites in the chip, 286 formed vias, and 2 formed septa.

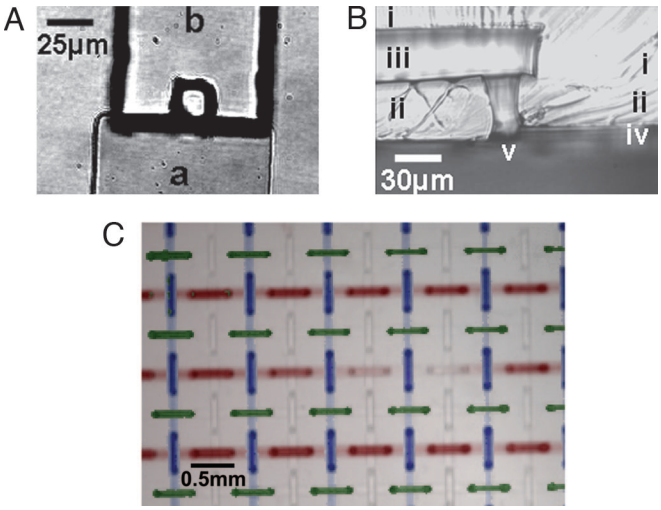

Fig. 4. Nonrounded vias form successfully over a wider spectrum of dimensions than rounded vias. The smallest functional nonrounded vias made to date are 25-μm square. (*A*) Top view shows lower (a) and upper (b) channels. (*B*) Side-view cross-section shows upper (i) and lower (ii) layers, upper (iii) and lower (iv) channels, and via (v). The chip was peeled off the slide, cut with a razor, and laid on its side to take the photograph. (*C*) A 4-plex design was executed with nonrounded vias at 2,500 rpm PDMS spin speed. The four-channel sets were filled with solutions containing plain buffer, fluorescein, Cy3, and Cy5 dyes; a colorless image and three false-color fluorescence images in blue, green, and red, respectively, were combined to produce the shown result. Of the 288 sites in the chip, 286 formed vias, and 2 formed septa (seen here at the ends of what would have been a red segment, mid-row, second from the right).

Nested Bioarrays

One of the applications of vias is printing bioarrays (22), e.g., protein or DNA arrays for immunoassays or hybridization expression analysis. As a particular example, we designed another chip containing four independent sets of 3D channels. Its primitive cell is a 4-plex (Fig. 5*A*), wherein each set accesses the substrate in one respective location. CRP (c-reactive protein) and ferritin monoclonal antibodies were each fed in a separate channel set and bound to the respective epoxide locations. We washed away the unbound excess with buffer, peeled off the PDMS chip, and passivated the unreacted epoxide with Tris buffer (14). We pipetted a mixture of CRP and ferritin antigens and fluorescently tagged polyclonal antibodies onto the slide. After incubation and washing, fluorescence detection led to the mixed false color image in Fig. 5*B*. The green (red) spots are produced by the Cy3 (Cy5) tag on the CRP (ferritin) polyclonal antibody, whereas the locations of the spots match the substrate access of the CRP (ferritin) monoclonal antibody, respectively. The results indicate the correct completion of the corresponding sandwich immunoassays.

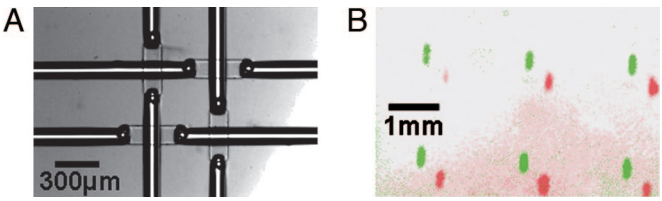

Fig. 5. Printing of nested bioarrays. We built a modified chip containing a 6×6 array of nested arrays (one is shown in *A*), wherein four nonmixing sets of channels access the substrate surface at one location each. CRP and ferritin monoclonal antibodies were each fed into a separate channel set and bound to the epoxide substrate, whereas the third and fourth sets were not used here. After washing away the excess, the chip was peeled off, and the rest of the epoxide was passivated with Tris buffer (14). A mixture of CRP and ferritin antigens and respective polyclonal antibodies tagged with Cy3 and Cy5 were incubated on the slide. (*B*) After another wash, fluorescence detection produced a false-color image demonstrating the correct assembly of the sandwich immunoassays of the nested bioarrays. If the initial substrate is diced after printing, this technique is a simple, fast, and inexpensive way to mass-produce identical nanomedicine chips, each conducting multiple tests on a separate sample. In principle, nested bioarrays of arbitrary size can be printed with three-layer devices (see *Nested Bioarrays*).

As Fig. 5*B* shows, the via technology provides a simple, fast, and inexpensive way to construct arrays of bioarrays (or "nested bioarrays"). To borrow an idea from the semiconductor industry, a large substrate wafer could thus be derivatized with complete parallelism and subsequently diced to yield a large number of identical microchips, each ready to be used for multiple tests on a separate sample. Such devices could form the centerpiece in a class of standardized inexpensive "nanomedicine chips" that could prove revolutionary in today's world of skyrocketing healthcare costs and mounting pressures for true personalized preventive medicine.

How large can the superarray and nested array be, as allowed by the underlying via technology? The 4-plex (Fig. 5) is a special case wherein underpasses double up as deposition access channels. If the number of individual reagents is increased, adjacent channels cannot jump over each other to create the superarray, unless they also access the substrate in extraneous locations.

To solve this problem, it is sufficient to increase the number of layers to three, wherein the first layer accesses the substrate, the second layer accommodates most of the length of the channels, and the third layer houses overpasses. This scheme can theoretically handle any number of individual reagents, and thus an arbitrary *n*-plex. The future should witness many important advances in patterning, as made possible by the presented microfluidic via technology.

Autoregulatory Devices

In the multilayer world of microfluidic valves (2, 3), vias remove the distinction between control and flow channels, because the same 3D channel can now be a control channel in one section of the chip and a flow channel in another. Therefore, the same 3D channel can act as a control channel on itself. This feature forms the basis of new autoregulatory devices.

Previous work in microfluidic autoregulation used the non-Newtonian rheological properties of concentrated polymeric solutions (26, 27). By contrast, the present work describes microfluidic autoregulation in Newtonian fluids, which has not been described previously, and thus in environments typical to most microfluidic applications.

Fig. 6 shows the simplest device architectures using pushup valves. In the pushup configuration, pressure applied to the channel in the lower layer deflects the valve membrane upward to pinch off the channel in the upper layer (3).

Within the "detour autoregulator" (Fig. 6*A*), static pressure decreases from source to exhaust as fluid flows along the main channel. Meanwhile, static pressure remains constant along the dead-end detour channel leading to the valve. Therefore, the pushup valve experiences an effective pressure equal to the static pressure drop between the channel split and the main-channel segment above the valve. Because of Poiseuille's law and geometry, that pressure drop scales with applied pressure. As the drop increases, the valve membrane deforms upward and constricts the main channel. Hence, total resistance increases with applied pressure, and the device behaves nonlinearly with Newtonian fluids.

The alternative architecture ("loop autoregulator") (Fig. 6*B*) utilizes the same pressure-drop principle. The loop eliminates the need for a detour channel but requires that the main channel

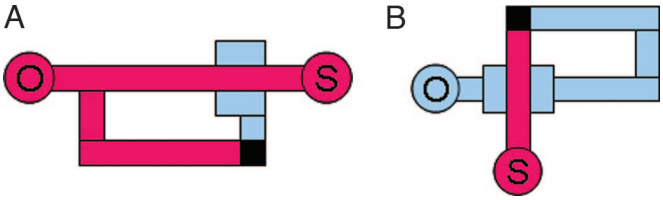

Fig. 6. Autoregulatory architectures. (*A*) In a detour autoregulator, pressure is applied at origin O to produce fluid flow along the main channel to exhaust/sink S, while a detour channel is connected to a pushup valve through a via (black). Channels in the upper and lower layers are drawn in red and blue, respectively. Static pressure decreases from origin to sink along the main channel due to the fluid flow, whereas the dead-end detour channel stays at the same static pressure as the split point. Thus, the pushup valve (3) experiences a pressure difference equal to the respective pressure drop, which scales with applied pressure due to Poiseuille's law. At sufficiently large applied pressures, the valve starts constricting the main channel, and the total resistance increases. Thus, the device behaves nonlinearly with Newtonian fluids. (*B*) A loop autoregulator utilizes the same pressure drop idea. The loop eliminates the need for a detour channel but requires that the main channel return to the starting point. Either architecture could be preferable in specific situations.

return to the starting point. Either architecture could be preferable in particular situations.

We constructed a set of detour autoregulators on the same chip, where the only varying parameter was the main-channel distance X between split and valve. All valves were 100×100 μm, all lower channels were 7×100 μm, and all upper channels were 26×100 μm in lateral dimensions. The length of all main channels was $L = 14.2$ mm. The autoregulator set had $X/L = \{0.80, 0.68, 0.57, 0.46, 0.23\}$. The 60-$\mu$m-square vias were rounded, and the PDMS was spun at 5,000 rpm. High-purity water was flowed through each device. Throughput (Fig. 7*A*) was measured by timing the advance of the water meniscus in transparent tubing connected to the exhaust. Larger split-to-valve distances monotonically correspond to lower saturation points, because identical valves experience larger percentages of the same total applied pressure. These experimental results offer a confirmation of the above qualitative predictions. They also demonstrate that the saturation throughput and saturation pressure of the device can be tuned by varying the split-to-valve length as a percentage of the main-channel length.

Fig. 7*B* shows the experimental results when the same detour autoregulator devices were used in reverse bias. Then, the effective pressure acts on the valve in the opening rather than closing direction and the devices act like plain channels. The small curvature upward in both forward and reverse bias is due to slight dilation of the elastomeric channels at higher pressures and the third-power dependence of throughput on the smaller lateral dimension in Poiseuille's law.

In forward bias, a detour autoregulator can be used alone as a microfluidic "current source" when operated in its saturation regime. Also, two such devices could be arranged back-to-back in series. Then each would act as a current source in its forward bias and as a plain channel in its reverse bias. An appropriately tuned design would ensure different saturation throughputs T in the different directions of applying pressure P. Thus, this compound device would be a previously undescribed type of a microfluidic "diode" (28).

Curiously, unlike the detour case, a loop autoregulator in reverse bias would act as a current source rather than as a plain channel. For example, the device in Fig. 6*B* would see a pressure drop applied on a pushup valve in forward bias and a pushdown valve in reverse bias, leading to saturation behavior in both directions. Careful engineering of the involved dimensions would produce an asymmetry between the saturation points of

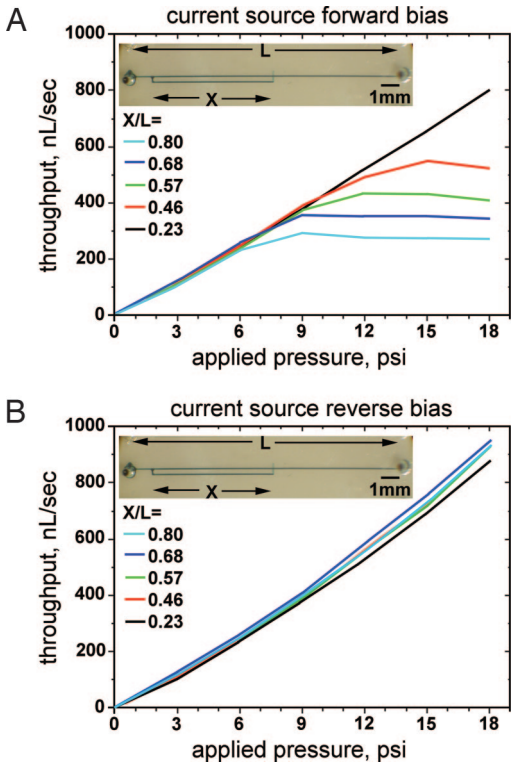

Fig. 7. Experimentally demonstrated current source. (*A*) Experimental results for the throughput as a function of applied pressure for a set of detour autoregulators (one is shown in the photograph), where the varying parameter was the distance X between split and valve. Larger X produced larger pressure drops for the same applied pressure, valve dimensions, and total main-channel length L. Thus, devices with larger X/L produced monotonically lower saturation points for throughput and pressure, demonstrating the predicted nonlinear behavior with Newtonian fluids. Hence, these devices can be used as microfluidic current sources with saturation characteristics that are tunable by architectural design. (*B*) The same devices then were reverse-biased by exchanging the roles of origin and sink. In reverse bias, the devices function linearly as plain channels. The small curvature upward is due to slight dilation of the elastomeric channels at higher pressures and the third-power dependence of throughput on the smaller lateral dimension in Poiseuille's law.

the two biases, thereby ensuring that the loop autoregulator would act as yet another type of a microfluidic diode.

The above detour and loop diodes could be used as building blocks to produce more advanced devices, such a microfluidic "rectifier" bridge, as is the case with their electronic counterparts. Although the correspondence between electrical and fluidic circuitry is not complete, analogies would prove useful. The above devices would form the basis of previously undescribed microfluidic analog logic in Newtonian fluids.

In conclusion, here we have presented a fundamental technological advance that enables large enhancements of the architectural complexity of 3D PDMS microfluidic devices by simple and easy means. The demonstrated applications are nested bioarrays and previously undescribed autoregulatory devices in Newtonian fluids.

Materials and Methods

Low Features on Thin-Layer Mold. Su8–2005 was spun at 1,000 rpm for 60 s with acceleration 15. The wafer was baked for 1 min at 65°C and 3 min at 95°C, exposed to UV for 40 s, baked again for 1 min at 65°C and 3 min at 95°C, developed in 100% Su8 developer for 20 s, rinsed in fresh developer, blown dry, and hard baked for 1 h at 150°C, with a 15-min ramp-up and ramp-down.

Thick-Layer Mold and High Features on the Thin-Layer Mold. The wafer was exposed to hexamethyldisilazane (HMDS) vapor for 90 s. Cold Az50 photoresist was spun at 1,400 rpm for 60 s at acceleration 15. The wafer was baked for 2, 5, and 2 min at 65, 115, and 65°C, respectively, exposed to UV for 4 min, developed in 3:1 water:2401 developer, rinsed in water, blown dry, and baked for 1 h at 200°C, with a 30 min ramp-up and ramp-down.

Chips and Experimental Setup. See ref. 14 and spin speeds in the text for details on the chips and experimental setup.

Labeling. CRP and ferritin antibodies (14) were respectively labeled with DyLight 547 and 647 NHS-Ester and then purified by using Zeba Desalt Spin Columns (exclusion limit, molecular weight 7,000), all from Pierce (Rockford, IL).

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